SN74LS74N

■ Product Introduction

The SN74LS74N is a D trigger with two sets of positive edge triggers. It has preset (Preset) and Clear function. The design of TTL output structure can be used as the interface of MCU control circuit.

■ Product Features

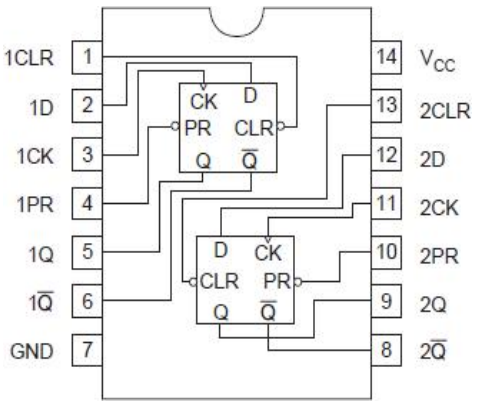
- D trigger with 2 sets of positive edge triggers
- It can be used as the interface of MCU control circuit.
- TTL circuit output design
- Input clamping diode to simplify system design
- With preset (Preset) and Clear function.
- Package : DIP14, SOP14

■ Product Applications

- Digital logic driver or Industrial control applications
- Other application areasBattery-powered equipment

■ Package and Pin Assignment

SOP14 or DIP14.			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Input 1CLR	14	Supply VCC
2	Input 1D	13	Input 2CLR
3	Input 1CK	12	Input 2D
4	Input 1PR	11	Input 2CK
5	Output 1Q	10	Input 2PR
6	Output 1Q	9	Output 2Q
7	Supply GND	8	Output 2Q



Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
welding temperature	T_W	260	℃,10s

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

Function Table

Inputs				Outputs	
PR	CLR	CK	D	Q	$\overline{Q}$
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

H:high level, L: low level, X: irrelevant, ↑ :transition from low to high level.

Q_0:level of Q before the indicated steady-state input conditions were established.

Q_0: complement of Q_0 or level of Q before the indicated steady-state input conditions were established.

*:This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Recommended Operating Conditions

Item		Symbol	Min	Tpy	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	-400	uA
		I_{OL}	—	—	8	mA
Operating temperature		T_A	0	—	60	℃
Pulse width	Clock	t_w	25	—	—	ns
	Clear、Preset	t_w	25	—	—	
Hold time		t_h	5↑	—	—	ns
Setup time	"H" Data	t_{su}	20↑	—	—	ns
	"L" Data	t_{su}	20↑	—	—	

Note: ↑ : The arrow indicates the rising edge.

Electrical Characteristics (T_A=25℃, Unless specified)

Item		Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage		V_{IH}	2	—	—	V		
		V_{IL}	—	—	0.7	V		
Output voltage		V_{OH}	2.7	3.3	—	V	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.7V, IOH = -400uA	
		V_{OL}	—	0.25	0.5	V	I_{OL} = 8 mA	V_{CC}=4.75V, V_{IL}=0.7V, V_{IH}=2V
			—	0.15	0.4		I_{OL} = 4 mA	
Input current	D	I_{IH}	—	—	20	uA	V_{CC} = 5.25V, V_I = 2.7V	
	Clear		—	—	40			
	Preset		—	—	40			
	Clock		—	—	20			
	D	I_{IL}	—	-0.13	-0.4	mA	V_{CC} = 5.25V, V_I = 0.4V	
	Clear		—	-0.20	-0.8			
	Preset		—	-0.20	-0.8			
	Clock		—	-0.20	-0.4			
	D	I_I	—	—	0.1	mA	V_{CC} = 5.25V, V_I = 7V	
	Clear		—	—	0.2			
	Preset		—	—	0.2			
	Clock		—	—	0.1			
Short-circuit output current *		I_{OS}	—	-35	-100	mA	V_{CC} = 5.25V	
Supply current **		I_{CC}	—	3.3	8	mA	V_{CC} = 5.25V	
Input clamp voltage		V_{IR}	—	-0.9	-1.5	V	V_{CC} =4.75 V, I_{IN}= -18 mA	

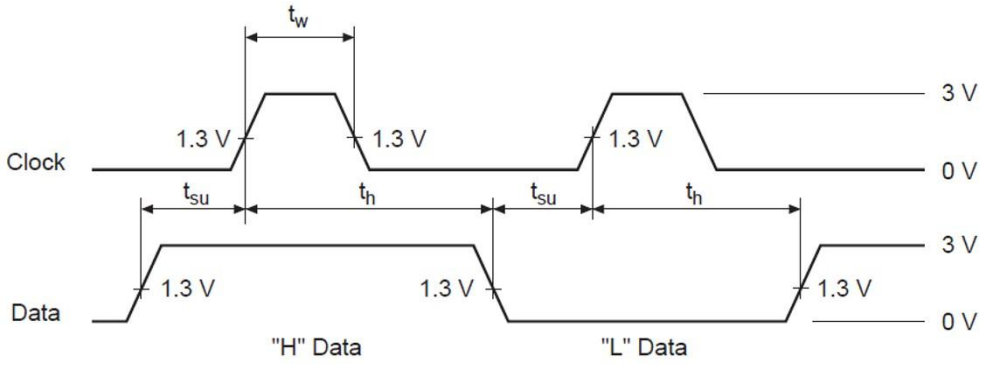
Note1: *only one output port is short circuited each time, and the short circuit time is not more than one second.

Note 2：**With all output open, Icc is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics (T_A=25℃, Unless specified)

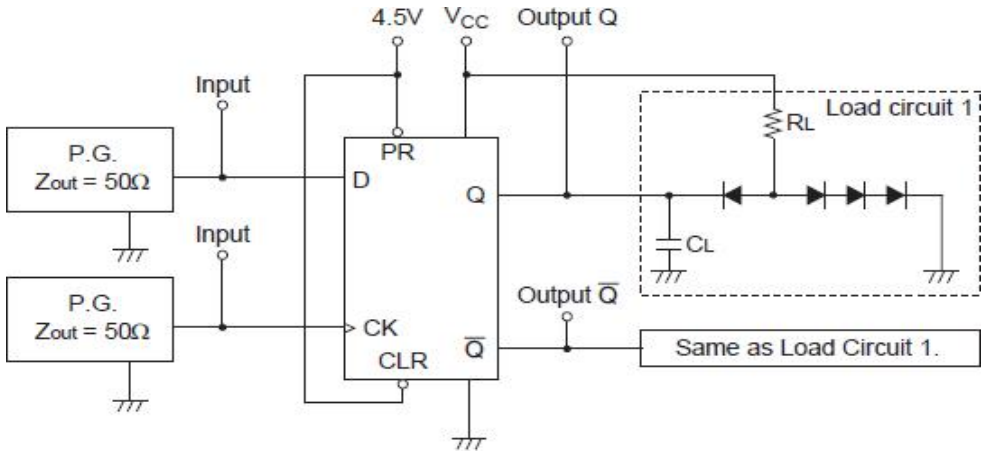
Item	Symbol	Input	Output	Min	Tpy	Max	Unit	Conditions
Propagation delay time	t_{PLH}	Clear、Clock or Preset	Q, $\overline{Q}$	—	22	40	ns	R_L=2k
	t_{PHL}			—	12	25	ns	C_L=15pF

Timing Definition



■ Testing Method

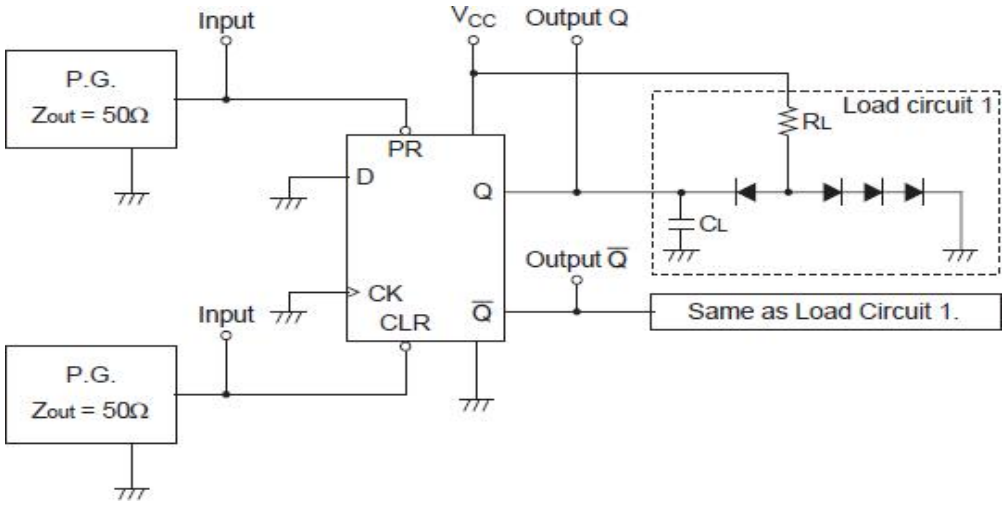
1、t_{PLH}、t_{PHL} (Clock→Q, $\overline{Q}$)



Notes:

1. Only one trigger is tested at a time.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
3. All diode models are 1S2074 (H).

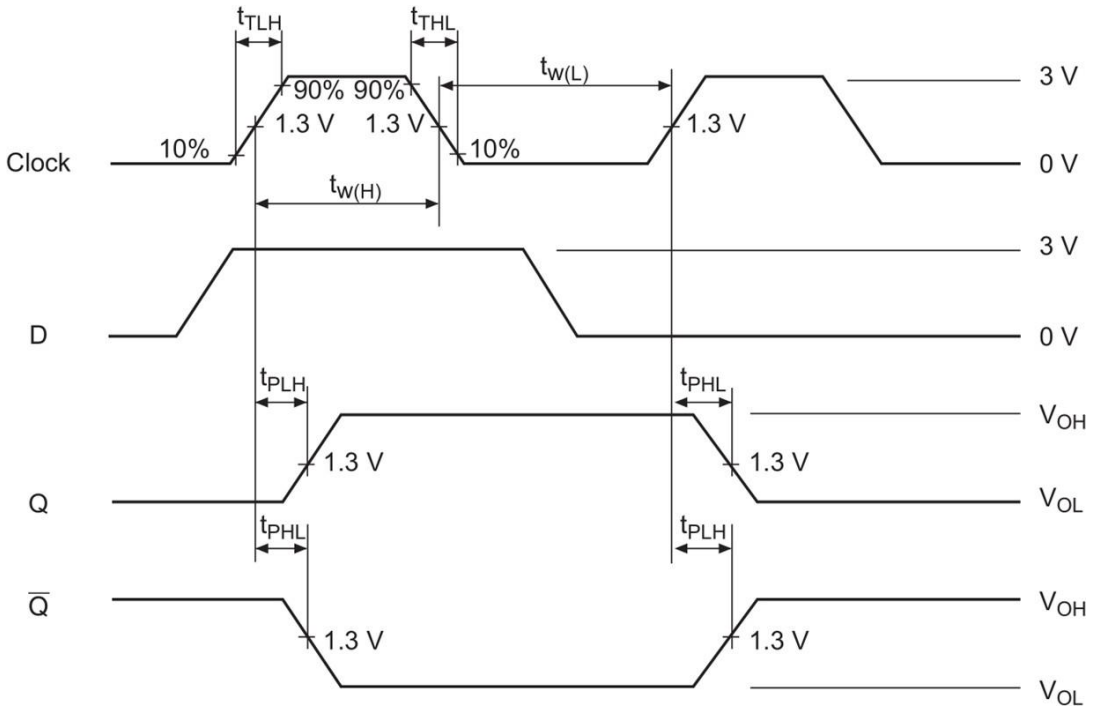
2、t_{PHL}, t_{PLH} (Clear or Preset→Q, $\overline{Q}$)



Notes:

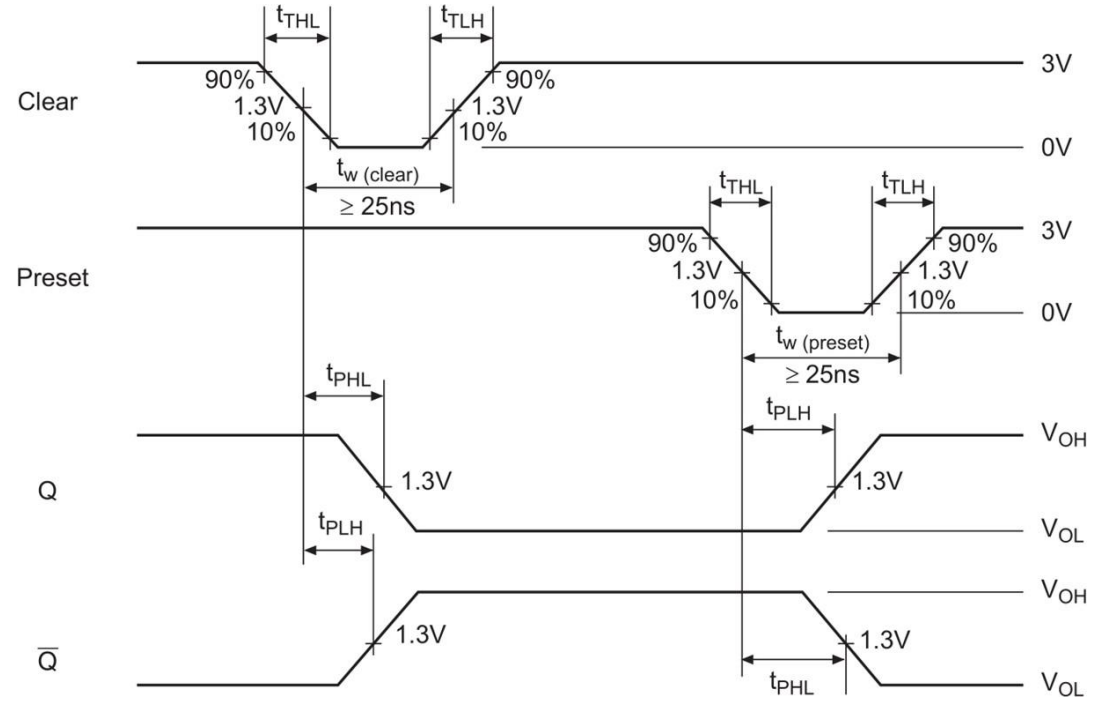
1. Only one trigger is tested at a time.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
3. All diode models are 1S2074 (H).

Waveform1：



Note: $t_{TLH} \leq 20$ ns, $t_{THL} \leq 20$ns, PRR = 1 MHz, duty cycle = 50%

Waveform2：

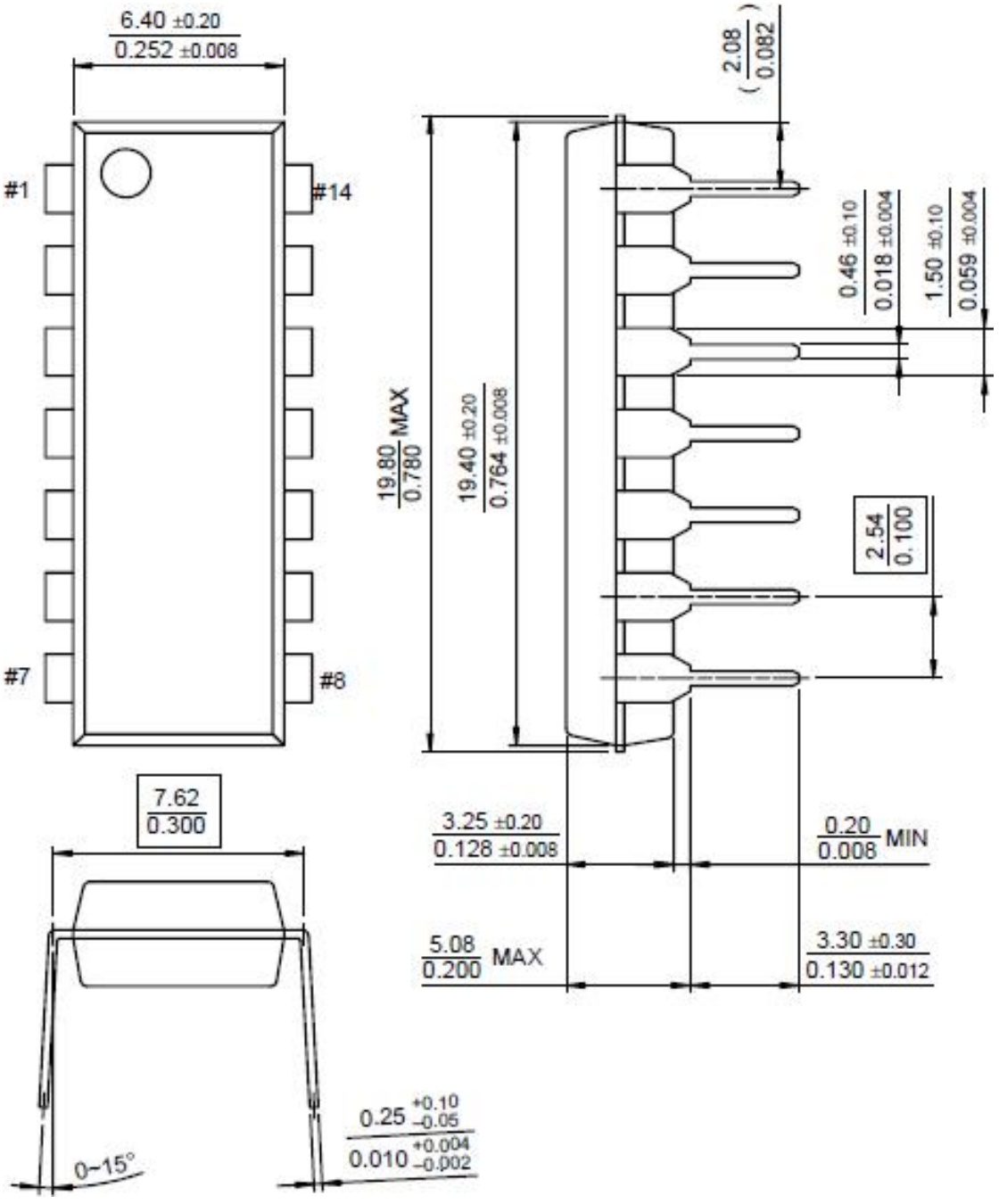


Note: $t_{TLH} \leq 20$ ns, $t_{THL} \leq 20$ns, PRR = 1 MHz, duty cycle = 50%

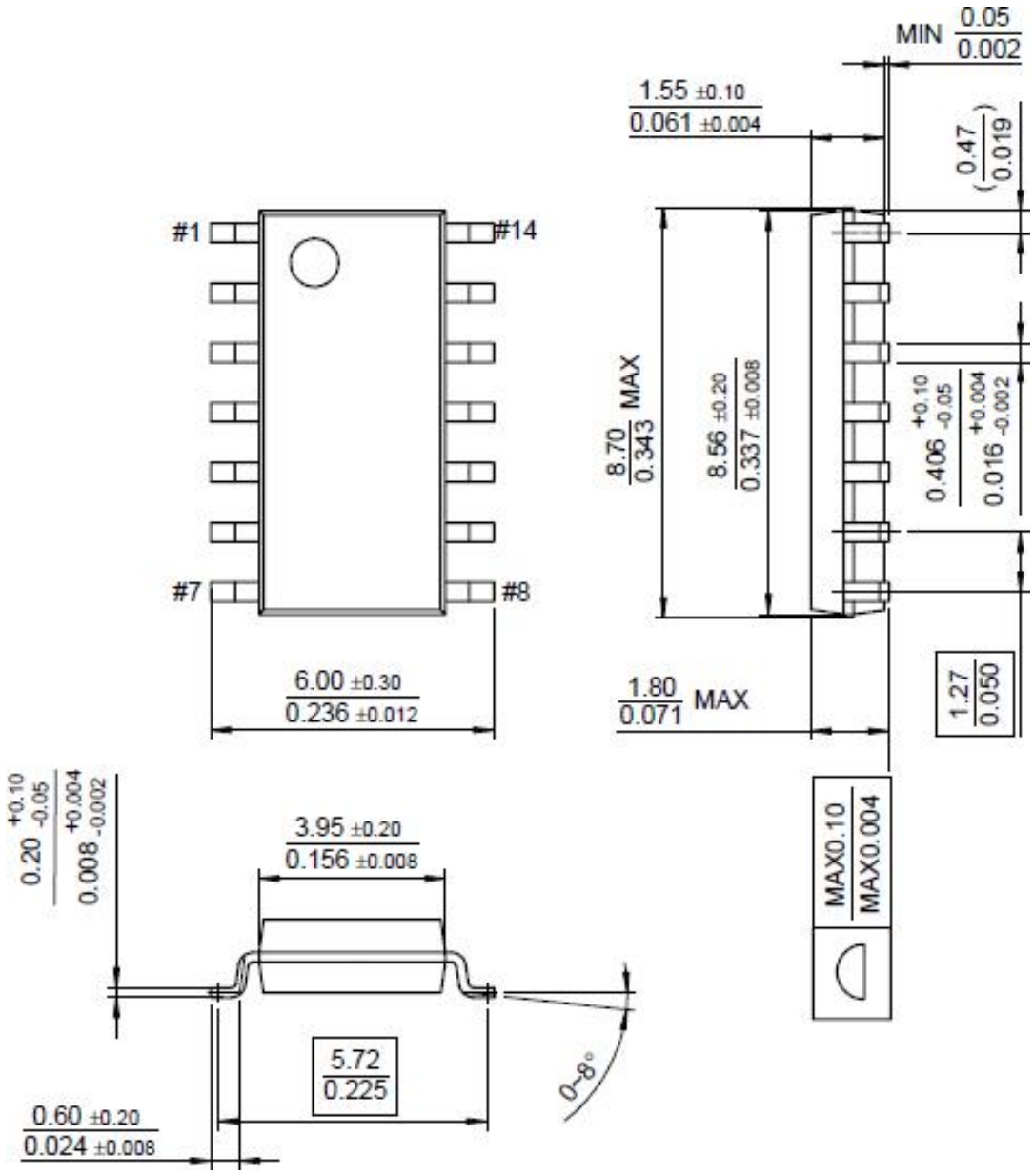
■ Package Dimensions

Unit：mm /inch

DIP14



SOP14


MIN 0.05 / 0.002
1.55 ±0.10 / 0.061 ±0.004
0.47 / 0.019
#1
#14
#7
#8
8.70 / 0.343 MAX
8.56 ±0.20 / 0.337 ±0.008
0.406 +0.10 -0.05 / 0.016 +0.004 -0.002
6.00 ±0.30 / 0.236 ±0.012
1.80 / 0.071 MAX
1.27 / 0.050
0.20 +0.10 -0.05 / 0.008 +0.004 -0.002
3.95 ±0.20 / 0.156 ±0.008
MAX0.10 / MAX0.004
5.72 / 0.225
0~8°
0.60 ±0.20 / 0.024 ±0.008